Frenkel (PF) emission, and TFE. Since the MOS-gate structure provides barrier height and thickness to suppress carrier transportation in the forms of TE and TFE, it is reasonable for MOSHFETs to have lower gate leakage at forward bias.

More importantly, the gate leakage current seem to show a very weak dependence on the device periphery as it is found to vary between 0.5 μA and 5.7 μA at V_{GS}=−10 V and in the range 3-19 μA under+2 V gate bias for gate width of 1-5 mm, still below the gate leakage current of 7 μA at −10V and 3 mA at 2V gate bias for the HFET with 0.25 mm gate width. This is due to the thin SiO2 gate dielectric layer. It is worth mentioning here that the subthreshold slope (SS) of MG MOSHFETs has not degraded (in FIG. **4**). J. W. Chung et al. observed that the SS is related to the gate leakage. The larger gate leakage makes SS worse. Due to the gate leakage suppression, large peripheries MOSHFETs SS have not degraded.

It was previously shown that the gate leakage current per unit area in AlGaN/GaN HFETs and AlInN/GaN MOSHFETs remains the same when either the gate width or gate length is varied, respectively. This was not the case for the devices studied in the present work. IGS was found to substantially increase when WG was increased from 250 μm to 1 mm, then no clear dependency with further increasing the gate width was observed. What is causing this behavior is still not well understood at this moment, but material and/or process non uniformity might be a factor. It is also known that the leakage current can originate from i) the parasitic leakage of the mesa regions or in the region where the gate feed runs over the mesa wall or ii) the presence of the SiN passivation layer which degrades the gate diode characteristics by introducing surface leakage current in the SiN layer or at its interface.

The three terminal off-state breakdown voltages were measured for several MOSHFET devices using the 1 mA/mm criteria. The gate-source bias applied was −6 V, which was about 2 V lower than the threshold voltage and no fluorinert solution, which usually prevents surface flashover and prevents to a premature device breakdown, was used. The breakdown voltage was found to be 110-137 V for the 0.15 mm devices and dropped down to 70 V for the large periphery MOSHFET with W_G~1 mm. Note that the surface passivation drastically increases the peak electric field at the drain side of the gate which can cause the local Schottky-barrier breakdown at the lower drain bias.

It is well known that the use of SiN passivation suppresses the rf dispersion for AlGaN/GaN HFETs by removing the surface states which relives the channel depletion as well. Therefore, with less surface states on the access region the higher ns−μ product is obtained to exhibit the higher $I_{DS,max}$ and g_{mMax}. However it also results in increase in gate-leakage currents. More investigation about the quality of gate dielectric and the effect and methods of reducing such leakage currents along with the study of the interface traps and defects are currently underway.

These and other modifications and variations to the present invention may be practiced by those of ordinary skill in the art, without departing from the spirit and scope of the present invention, which is more particularly set forth in the appended claims. In addition, it should be understood the aspects of the various embodiments may be interchanged both in whole or in part. Furthermore, those of ordinary skill in the art will appreciate that the foregoing description is by way of example only, and is not intended to limit the invention so further described in the appended claims.

What is claimed:

1. A method of forming a semiconductor field-effect transistor, the method comprising:

forming a multilayer stack on the substrate, wherein the multilayer stack comprises a group III nitride epilayer, a back barrier layer, and a spacer layer;

forming a ultra-thin barrier layer on the multilayer stack, wherein the ultra-thin barrier layer has a thickness of about 0.5 nm to about 10 nm;

forming a dielectric, discontinuous thin film layer comprising SiO_2 on portions of the ultra-thin barrier layer while leaving other portions exposed;

forming a plurality of source electrodes and drain electrodes on the exposed areas of the ultra-thin barrier layer in an alternating pattern such that the dielectric, discontinuous thin film layer is positioned between adjacent source electrodes and drain electrodes; and

forming gate electrodes on the dielectric, discontinuous thin film layer.

2. The method of claim **1**, further comprising:

forming a gate interconnection to electrically connect the gate electrodes.

3. The method of claim **2**, further comprising:

forming a passivation layer on the device.

4. The method of claim **3**, further comprising:

forming a source interconnection to electrically connect the source electrodes; and

forming a drain interconnection to electrically connect the drain electrodes, wherein the source electrodes and the drain electrodes are electrically isolated from each other.

5. The method of claim **1**, wherein the source electrodes and the drain electrodes have an interlaced source-gate drain electrode structure.

6. The method of claim **1**, wherein the substrate comprises sapphire, and wherein the multilayer stack comprises a group III nitride epilayer, a back barrier layer, and a spacer layer.

7. The method of claim **6**, wherein the group III nitride epilayer comprises $Al_xIn_yGa_{1-x-y}N$, where $0\leq x\leq 1$, $0\leq y\leq 1$ and $0<x+y\leq 1$, and wherein the back barrier layer comprises $Al_xIn_yGa_{1-x-y}N$, where $0\leq x\leq 1$, $0\leq y\leq 1$ and $0\leq x+y\leq 1$.

8. The method of claim **6**, wherein the group III nitride epilayer comprises GaN, and wherein the back barrier layer GaN.

9. The method of claim **6**, wherein the spacer layer comprises $Al_xIn_yGa_{1-x-y}N$, where $0\leq x\leq 1$, $0\leq y\leq 1$ and $0<x+y\leq 1$.

10. The method of claim **1**, wherein the ultra-thin barrier layer comprises $Al_xIn_yGa_{1-x-y}N$, where $0\leq x\leq 1$, $0\leq y\leq 1$ and $0<x+y\leq 1$.

11. The method of claim **1**, wherein the ultra-thin barrier layer comprises AlInN.

12. The method of claim **1**, wherein the ultra-thin barrier layer has a thickness of about 0.5 nm to about 10 nm.

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